WHAT IS CLAIMED IS:

1. A method for defining a system specification for a digital system, said method comprising the steps of:

partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;

defining a data communication protocol for communication between said processes;

configuring data communication interfaces in the form of communication input ports and communication output ports for each of the processes, the communication ports forming memoryless communication channels; and

combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.

2. The method of Claim 1, wherein the specification for a first process is independent of the specification of a second process.

3. The method of Claim 1, further comprising the step of duplicating the specification for a process of a first system for a process of a second system.

4. The method of Claim 1, wherein said step of configuring data communication interfaces involves defining communication interfaces with input ports and output ports to provide unidirectional, point-to-point connections between input ports of a first process and output ports of a second process, said input ports and said output ports being part of the associated processes.

5. The method of Claim 4, wherein defining interfaces having output ports comprises the steps of:

defining a data terminal having a plurality of input signal lines;

defining a strobe terminal having at least one input signal line; and

defining an acknowledge terminal having at least one output signal line.

6. The method of Claim 4, wherein defining interfaces having output ports comprises the steps of:

defining a data terminal having a plurality of output signal lines;

defining a strobe terminal having at least one output signal line; and

defining an acknowledge terminal having at least one input signal line.

7. The method of Claim 4, further comprising of step of defining said processes to synchronize at communication instants.

8. The method of Claim 4, wherein said ports are defined with a blocked protocol whereby the control flow of a process is halted until the process associated with the port is synchronized.

9. The method of Claim 5, wherein said ports are defined with an unblocked protocol whereby the control flow of a process is continues regardless of whether the process associated with the port is synchronized.

10. The method of Claim 4, wherein the communication protocol comprises a four-phase handshake protocol.

11. The method of Claim 4, wherein said step of partitioning comprises defining a plurality of processes as a single process.

12. The method of Claim 4, wherein said processes are implemented in a hardware description language or in a programming language.

13. The method of Claim 12, wherein said processes are implemented in C, Silage or VHDL language.

14. A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining a data communication protocol for communication between said processes;

organizing said data communication protocol with input and output ports for said processes, said ports using defining memoryless communication channels; and

specifying processors to implement said processes.

15. The method of Claim 14, wherein said step of designing processors comprises the step of specifying a processor having specification which conform to to the processes implemented.

16. The method of Claim 15, wherein said processor comprises a programmable, general purpose processor.

17. The method of Claim 15, wherein said processor comprises a programmable digital signal processor.

18. The method of Claim 15, wherein said processor comprises a dedicated, custom processor.

19. The method of Claim 15, wherein said processor comprises custom logic circuit with a controller such that the resulting digital system operates according to functional and real-time specifications.

20. The method recited in Claim 15, wherein said ports and communication channels are implemented as shared memory.

21. The method recited in Claim 15, wherein said ports and communication channels are implemented as sockets.

22. The method recited in Claim 15, wherein said ports and communication channels are implemented files.

23. The method recited in Claim 15, wherein said ports and communication channels are implemented a mailbox.

24. The method recited in Claim 15, wherein said ports and communication channels are implemented in the operating system of a multi-process operating system for simulating the system processes and communications channels on a multi-processing computer.

25. The method recited in Claim 15, wherein said ports and communication channels are implemented in the operating system of a multi-process operating system for simulating the system processes and communications channels on a network of computers

26. The method recited in Claim 15, wherein said ports and communication channels are implemented in the operating system of a multi-process operating system for simulating the system processes and communications channels in a multi-tasking implementation shell.

27. The method of Claim 15, wherein said communication ports connect processes defined of at least one of a plurality of specifications.

28. The method of Claim 27, wherein said plurality of specifications are selected from a group consisting of silage descriptions, C descriptions, VHDL process descriptions.

29. The method of Claim 15, wherein said communication channels are implemented as memory mapped I/O.

30. The method of Claim 15, wherein said communication channels are implemented as interrupt driven I/O.

31. The method recited in Claim 16, wherein said communication channels are implemented in integrated circuit form for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

32. The method of Claim 35, wherein said plurality of processor types consists of cathedral-III processors, ARM processors and VHDL processors.

33. The method recited in Claim 16, wherein said communication channels are implemented in software for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

34. The method recited in Claim 16, wherein said communication channels are implemented in a combination of hardware and software, for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

35. The method recited in Claim 17, wherein said step of partitioning involves defining a library of auxiliary processes to simulate the digital system, the library of processes selected from a plurality of processes.

36. The method of Claim 35, wherein said plurality of processes consists of one or more of an interactive I/O process, a file I/O process, a graphical output process, a channel duplicator process, a channel merging process, a FFT process, a slider process, a button process, a first-in, first-out buffer process, an ARM processor, a digital to analog conversion process and an analog to digital conversion process.

37. A system for receiving signals developed using the method of Claim 18, comprising:

a receiver chain with a down-converter;

a receive filter;

a gain control circuit;

a clock generator for said receiver chain;

means for programming said receiver chain and said clock generator; and

a processor for pilot demodulation, traffic demodulation and noise estimation.

38. The system of Claim 42, wherein said system is realized as an integrated circuit.

39. A system for transmitting and receiving signals devloped in accordance with the method of Claim 18, comprising:

a digital integrated circuit comprising a transmitter with a first chain of hardware blocks generating first baseband signals, a converter to serialize input data signals, a spreader, an over-sampling filter, a gain control facility, and an up-converter to convert said baseband signals to first signals at an intermediate frequency;

a receiver with a second chain of hardware blocks generating a plurality of output data signals, comprising a down-converter to convert second signals at an intermediate frequency to second baseband signals, a decimating filter, a gain control facility, and a correlator block generating said plurality of output data signals;

a clock generator with a numerically controlled oscillator generating a clock for said transmitter, and a numerically controlled oscillator generating a clock for said receiver;

means for programming said digital integrated circuit;

a module measuring the phase error between an external signal and one of said plurality of output data signals;

a processor for writing parameters to said digital integrated circuit and for reading said plurality of output data signals and said phase error to said processor; and

means to interface said circuit to said processor using memory mapped input/output.

40. The system of Claim 43, wherein said system is realized as an integrated circuit.

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